IN THE SPECIFICATION

Please amend the paragraphs identified below to read as follows:

[0056] 2. Alternatively, the surfaces of the SOI N+/P+ doped well regions 33L/33R can be treated with a monolayer of dopant diffusion retardation agent such as Si-O-CH_3 methoxy termination; an alkyl termination; silicon carbide (SiC) grown in situ; or silicon Germanium (SiGe) grown in situ. The dopant diffusion retardation coating produced, which is to serve as the dopant diffusion retarding barrier 47L/47R must be maintained relatively thin (less than a single nm or a few nm) in order to permit subsequent growth of epitaxial silicon on the surface thereof with the lattice structure of the underlying SOI N+/P+ doped well regions 33L/33R.

[0062] FIG. 3M shows the device 30 of FIG. 3L after formation of ultra-thin intrinsic epitaxial regions 48L/48R having a thickness between about 5 nm and about 15 nm which are to be employed as intrinsic channel regions over the highly doped SOI N+/P+ doped well regions 33L/33R respectively. The epitaxial regions 48L/48R are grown anisotropically vertically, aside from the isolation region 39, by a process of RTCVD (Rapid Thermal Chemical Vapor Deposition) based upon the crystalline structure of the SOI regions 33L/33R.

[0064] FIG. 3O shows the device 30 of FIG. 3N after formation of PFET and NFET devices including P+ gate electrode 54P and N+ gate electrode 54N above the gate dielectric layer 50, with upper drain regions 55L/55R and source regions 56L/56R juxtaposed with the channel regions CH in epitaxial regions 48L/48R aside from the gate electrodes 54P/54N. There are lower drain regions 55L'/55R' and lower source regions 56L'/56R' formed in the doped well regions 33L/33R which include ground planes ~~33L/33R~~ respectively below the gate electrodes 54P/54N respectively. The lower source regions 55L'/55R' and the lower drain regions 56L'/56R' are shown reaching down to the buried oxide layer 32 through the heavily doped SOI/ground plane/doped well regions 33L/33R, ensuring a minimized junction area. Therefore junction capacitance and leakage are minimized. The channel regions CH are formed in the intrinsic epitaxial regions 48L/48R and thus, as in FIG. 3N, they are located above the N+/P+ highly doped SOI/ doped well regions 33L/33R which include ground planes therein. ~~33L/33R.~~ Silicide contacts 69 are provided to the source/drains regions 56/55. Silicide regions 54P'/54N' are formed above the gate electrodes 54P/54N. Silicon oxide extension spacers 52, dielectric sidewall spacers SP and TEOS/Source Drain spacers 53 can be formed aside from the gate electrodes 54.

[0070] In step 74, an oxide liner 38 is formed in the isolation trench 37 on the sidewalls of the SOI well regions 33L/33R as shown in FIG. 3F.

[0072] In step 76, a sacrificial layer 40L/40R of silicon oxide or the like is formed on the top surfaces of the SOI well regions 33L/33R in FIG. 3H.

[0073] Next, as illustrated by FIG. 3I, a mask 42 is formed over the top surface of the sacrificial layer 40R to protect the SOI region 33R; and N-type dopant is ion implanted into the left SOI well region 33L to a high N+ doping level as described above with reference to FIG. 3I.

[0074] Next, as illustrated by FIG. 3J, the mask 42 is stripped and another mask 45 is formed over the top surface of the sacrificial layer 40L to protect the SOI, N+ doped well region 33L; and P-type dopant is ion implanted into the right SOI well region 33R to a high P+ doping level as described above with reference to FIG. 3J.

[0077] In step 78, ultra-thin intrinsic epitaxial regions 48L and 48R having a thickness ranging from about 5 nm to about 15 nm are formed above the SOI well regions 33L and 33R respectively as shown in FIG. 3M.

[0087] In step 96, a sacrificial layer 40L/40R of silicon oxide or the like is formed on the top surfaces of the SOI well regions 33L/33R in FIG. 3H.

[0088] Next, as illustrated by FIG. 3I, a mask 42 is formed over the top surface of the sacrificial layer 40R to protect the SOI well region 33R; and N-type dopant is ion implanted into the left SOI well region 33L to a high N+ doping level as described above with reference to FIG. 3I.

[0089] Next, as illustrated by FIG. 3J, the mask 42 is stripped and another mask 45 is formed over the top surface of the sacrificial layer 40L to protect the SOI well region 33L; and P-type dopant is ion implanted into the right SOI well region 33R to a high P+ doping level as described above with reference to FIG. 3J.

[0091] In step 98, as indicated by FIG. 3L, a dopant diffusion retarding barrier 47L/47R is formed over the highly doped SOI well regions 33L/33R.

[0094] 1. To form the dopant diffusion retarding barrier 47L/47R, the top surfaces of the well regions 33L/33R are treated with co-implantation of doping diffusion retarding ions into the top surface of the well regions 33L/33R. Examples of such ions are carbon (C) germanium (Ge) and/or xenon (Xe) into the top surface of the 33L/33R layers.

[0095] 2. Alternatively, the surfaces of the SOI well regions 33L/33R can be treated with a monolayer of dopant diffusion retardation agent such as Si-O-CH_3 methoxy termination, an alkyl termination, or silicon carbide (SiC) grown in situ, or silicon Germanium (SiGe) grown in situ. The dopant diffusion retardation coating produced, which is to serve as the dopant diffusion retarding barrier 47L/47R must be maintained relatively thin (less than a single nm or a few nm) in order to permit subsequent growth of epitaxial silicon on the surface thereof with the lattice structure of the underlying SOI regions 33L/33R.

[0096] In step 99 ultra-thin intrinsic epitaxial regions 48L and 48R having a thickness ranging from about 5 nm to about 15 nm are formed above the SOI well regions 33L and 33R respectively as shown in FIG. 3M.